AMENDMENT

To the Specification:

Please amend the specification as follows:

[0009] The present invention provides a circuit for enhancing motion picture quality, comprising: a first dual-port buffer for receiving and temporarily storing a first frame data, and first-in-first-out outputting the first frame data; a second dual-port buffer for receiving and temporarily storing a second frame data, and first-in-first-out outputting the second frame data; the first frame data being shown in a motion picture after the second frame data; a frame memory for storing a motion picture data; a multiplexer unit, coupled to said first dual-port buffer, said second dual-port buffer, and said frame memory, for selecting and transmitting one of said outputted said first frame data to said frame memory and said outputted said second frame data from said frame memory to said second dual-port buffer; and a ~~signal-converter~~signal-converter for obtaining a compensation data to output a third frame data in response to the first frame data and the second frame data corresponding to the first frame data.

[0010] In a preferred embodiment of the present invention, the circuit further comprises: a first data latch for receiving a fourth frame data and outputting the first frame data, wherein the number of bits of the first frame data is larger than the number of bits of the fourth frame data; a second data latch for receiving a fifth frame data and outputting the second frame data, wherein the number of bits of the second frame data is larger than the number of bits of the fifth frame data; wherein the ~~signal-converter~~ signal-converter obtains the compensation data to output the third frame data in response to the fourth frame data and the fifth frame data corresponding to the second

frame data.

[0011] In a preferred embodiment of the present invention, the circuit further comprises a nonlinear quantizer for receiving a sixth frame data and quantizing the sixth frame data by using a nonlinear quantization method to output the fourth frame data, wherein the ~~signal-converter~~signal-converter is for receiving the sixth frame data and compensating the sixth frame data based on the compensation data to obtain the third frame data.

[0012] The present invention provides a circuit for enhancing motion picture quality, comprising: a nonlinear quantizer for receiving a first frame data and quantizing the first frame data by using a nonlinear quantization method to output a second frame data; a frame memory module, coupled to the nonlinear quantizer, for receiving the second frame data and outputting a third frame data corresponding to the second frame data, the second frame data being shown in a motion picture after the third frame data; and a ~~signal-converter~~signal-converter, in response to the second frame data and the third frame data corresponding to the second frame data, for obtaining a compensation data to compensate the first frame data for outputting a fourth frame data.

[0013] In a preferred embodiment of the present invention, the frame memory module comprises: a first dual-port buffer for receiving and temporarily storing the second frame data, and first-in-first-out outputting the second frame data; a second dual-port buffer for receiving and temporarily storing the third frame date, and first-in-first-out outputting the third frame data; a frame memory for storing a motion

picture data; and a multiplexer unit coupled to said first dual-port buffer, said second dual-port buffer and said frame memory; for selecting and transmitting one of said outputted said second frame data to said frame memory and said outputted said third frame data [[to]]from said frame memory to said second dual-port buffer.

[0014] In a preferred embodiment of the present invention, the ~~signal converter~~ signal-converter comprises: a motion picture enhancing unit for simultaneously receiving the second frame data and the third frame data and comparing the second frame data and the second frame data to generate the compensation data based on the difference between the second frame data and the third frame data; and a data processing unit for simultaneously receiving the first frame data and the compensation data corresponding to the first frame data, and compensating the first frame data based on the compensation data to obtain the fourth frame data.

[0015] The present invention provides a method for enhancing motion picture quality, comprising: providing a first dual-port buffer, a second dual-port buffer, and a frame memory; using the first dual-port buffer to receive and temporarily store a first frame date, and first-in-first-out outputting the first frame data; using the second dual-port buffer to receive and temporarily store a second frame date, and first-in-first-out outputting the second frame data; the first frame data being shown in a motion picture after the second frame data; using the frame memory to store a motion picture data; multiplexing said motion picture data in said frame memory thereby selecting and transmitting one of said outputted said first frame data to said frame memory and said outputted said second frame data from said frame memory to said

second dual-port buffer; and obtaining a compensation data to output a third frame data in response to the first frame data and the second frame data corresponding to the first frame data.

[0016] The present invention provides a circuit for enhancing motion picture quality, comprising: a first dual-port buffer for receiving and temporarily storing a first frame date, and first-in-first-out outputting the first frame data; a second dual-port buffer for receiving and temporarily storing a second frame date, and first-in-first-out outputting the second frame data; the first frame data being shown in a motion picture after the second frame data; a frame memory for storing a motion picture data; a multiplexer unit, coupled to said first dual-port buffer, said second dual-port buffer, and said frame memory, for selecting and transmitting one of said outputted said first frame data to said frame memory and said outputted said second frame data from said frame memory to said second dual-port buffer; a ~~signal-converter~~signal-converter, in response to the first frame data, a third frame data, and the second frame data corresponding to the third frame data, for obtaining a compensation data to output a fourth frame data and a fifth frame data; a first data flow switcher receiving a sixth frame data and a seventh frame data and transforming the sixth frame data and the seventh frame data into one of the first frame data and the third frame data respectively and the third frame data and the first frame data respectively; and a second data flow switcher for receiving the fourth frame data and the fifth frame data and transforming the fourth frame data and the fifth frame data into one of the eighth frame data and the ninth frame data respectively and the eighth frame data and the ninth frame data respectively.

[0017] In a preferred embodiment of the present invention, the circuit further comprises a first data latch, coupled to and between the first data flow switcher and the first dual-port buffer, the first data flow switcher receiving the sixth frame data and the seventh frame data, and transforming the sixth frame data and the seventh frame data into one of a tenth frame data and the third frame data respectively and the third frame data and the tenth frame data respectively, the first data latch for receiving the tenth frame data and outputting the first frame data, the number of bits of the first frame data is larger than the number of bits of the tenth frame data; a second data latch, coupled to and between the first dual-port buffer and the ~~signal converter~~signal-converter, receiving the second frame data and outputting an eleventh frame data, the number of bits of the second frame data is larger than the number of bits of the eleventh frame data; wherein the ~~signal converter~~signal-converter, in response to the tenth frame data, the third frame data, and the eleventh frame data corresponding to the third frame data, obtaining the compensation data to output the fourth frame data and the fifth frame data.

[0018] In a preferred embodiment of the present invention, the circuit further comprises: a first nonlinear quantizer, coupled to and between the first data flow switcher and the first data latch, the first data flow switcher for receiving the sixth frame data and the seventh frame data, and transforming the sixth frame data and the seventh frame data into one of a twelfth frame data and the third frame data respectively and the third frame data and the twelfth frame data respectively, the first nonlinear quantizer for receiving the twelfth frame data and quantizing the twelfth frame data by using a nonlinear quantization method to output the tenth frame data; and a second nonlinear quantizer, coupled to and between the first data flow switcher and the ~~signal converter~~

signal-converter, receiving the third frame data and quantizing the third frame data by using a nonlinear quantization method to output the thirteenth frame data; wherein the ~~signal-converter~~signal-converter, in response to the twelfth frame data, the third frame data, and the thirteenth frame data corresponding to the eleventh frame data, obtains the compensation data to output the fourth frame data and the fifth frame data.

[0019] The present invention provides a circuit for enhancing motion picture quality, comprising: a first nonlinear quantizer for receiving a first frame data and quantizing the first frame data by using a nonlinear quantization method to output a second frame data; a second nonlinear quantizer for receiving a third frame data and quantizing the third frame data by using a nonlinear quantization method to output a fourth frame data a frame memory module, coupled to the first nonlinear quantizer, for receiving the second frame data and outputting a fifth frame data corresponding to the second frame data, the second frame data being shown in a motion picture after the fifth frame data; a ~~signal converter~~signal-converter, in response to the first frame data, the third frame data, the fourth frame data and the fifth frame data corresponding to the fourth frame data, for obtaining a compensation data to output a sixth frame data and a seventh frame data; a first data flow switcher for receiving an eighth frame data and a ninth frame data and transforming the eight frame data and the ninth frame data into one of the first frame data and the third frame data respectively and the third frame data and the first frame data respectively; and a second data flow switcher for receiving the sixth frame data and the seventh frame data and transforming the sixth frame data and the seventh frame data into one of the tenth frame data and the eleventh frame data respectively and the tenth frame data and the eleventh frame data respectively.

[0020] In a preferred embodiment of the present invention, the frame memory module comprises: a first dual-port buffer for receiving and temporarily storing the second frame date, and first-in-first-out outputting the second frame data; a second dual-port buffer for receiving and temporarily storing the fifth frame date, and first-in-first-out outputting the fifth frame data; a frame memory for storing a motion picture data; and a multiplexer unit coupled to said first dual-port buffer, said second dual-port buffer, and said frame memory; for selecting and transmitting one of said outputted said second frame data to said frame memory and said outputted said fifth frame data from said frame memory to said second dual-port buffer.

[0021] The present invention provides a method for enhancing motion picture quality, comprising: providing a first dual-port buffer, a second dual-port buffer, and a frame memory; using the first dual-port buffer to receive and temporarily store a first frame date, and first-in-first-out outputting the first frame data; using the second dual-port buffer to receive and temporarily store a second frame date, and first-in-first-out outputting the second frame data; the first frame data being shown in a motion picture after the second frame data; using the frame memory to store a motion picture data; multiplexing said motion picture data in said frame memory thereby selecting and transmitting one of said outputted said first frame data to said frame memory and said outputted said second frame data from said frame memory to said second dual-port buffer; and obtaining a compensation data to output a fourth frame data and a fifth frame data, in response to the first frame data, a third frame data, and the second frame data corresponding to the third frame data; transforming a sixth frame

data and a seventh frame data into one of the first frame data and the third frame data respectively and the third frame data and the first frame data respectively, in response to a time sequence; and transforming the fourth frame data and the fifth frame data become one of an eighth frame data and a ninth frame data respectively and the ninth frame data and the eighth frame data respectively, in response to the time sequence.

[0039] In a second embodiment of the present invention, even if the nonlinear quantizer 610 and the motion picture enhancing unit 652 in FIG. 6 are not used so that the frame data 602 and 611 are the same signal, and the frame data 641 and 651 are the same signal, this circuit is still within the scope of the present invention. In a third embodiment of the present invention, the circuit omits the data latches 620 and 640 in the second embodiment, this circuit is still within the scope of the present invention. In addition, the ~~signal-converter~~signal-converter 650 can also be replaced by the other units in the above embodiments.

[0048] In a seventh embodiment of the present invention, even if the nonlinear quantizers 720 and 730, and the motion picture enhancing unit 772 in FIG. 7 are not used so that the frame data 713 and 721 are the same signal, and the frame data 761 and 771 are the same signal, this circuit is still within the scope of the present invention. In an eighth embodiment of the present invention, the circuit omits the data latches 740 and 760 in the seventh embodiment, the frame data 713 and 741 are the same signal and the frame data 757 and 761 are the same signal; this circuit is still within the scope of the present invention. In addition, the ~~signal-converter~~signal-converter 770 can also be replaced by the other units in the above embodiments.